4K I²C Serial EEPROM with Software Write Protection

FEATURES

- Low voltage and low power operations:
  - FT34C04A: VCC = 1.7V to 3.6V, Industrial temperature range (-40℃ to 85℃).
- JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) Compliant
- Individually reversible software write protection on all four 128-byte quadrants.
- 16 bytes page write mode.
- Partial page write operation allowed.
- Industy standard 100kHz, 400 kHz,and 1MHz I²C interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed programming cycle (5ms maximum).
- Bus Timeout Supported
- Automatic erase before write operation.
- High reliability: typically 1,000,000 cycles endurance.
- 100 years data retention.
- Standard 8-lead JEDEC SOP, 8-lead TSSOP, and 8-pad UDFN Pb-free packages.

DESCRIPTION

The FT34C04A is a 1.7V rated minimum operating voltage Serial EEPROM device containing 4096-bits of Serially Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 512-bytes of eight bits each. The Serial EEPROM operation is tailored specifically for DRAM memory modules with Serial Presence Detect (SPD) to store a module's vital product data such as the module's size, speed, voltage, data width, and timing parameters.The FT34C04A is protocol compatible with the legacy JEDEC EE1002 specification (2-Kbit) devices enabling the FT34C04A to be utilized in legacy applications without any software changes. The device is designed to respond to specific software commands that allow users to identify and set which half of the memory the internal address counter is located. This special page addressing method to select the upper or lower half of the Serial EEPROM is what facilitates legacy compatibility. However, there is one exception to the legacy compatibility as the FT34C04A does not support the Permanent Write Protection feature.Additionally, the FT34C04A incorporates a Reversible Software Write Protection (RSWP) feature enabling the capability to selectively write protect any or all of the four 128-byte quadrants. Once the RSWP is set, it can only be reversed by sending a specific software command sequence.The FT34C04A supports the industry standard 2-wire I2C Fast-Mode Plus (FM+) serial interface allowing device communication to operate at up to 1MHz. A bus timeout feature is supported to help prevent system lock-ups. The FT34C04A is available in space saving SOP, TSSOP, and UDFN packages.

PIN CONFIGURATION

Pin Name	Pin Function
A2, A1, A0	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
NC	No-Connect
VCC	Power Supply
GND	Ground

Table 1

All these packaging types come in conventional or Pb-free certified.

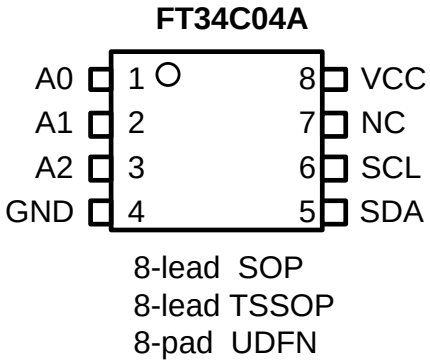


Figure 1: Package types

ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40℃ to 85℃
Storage temperature:	-50℃ to 125℃
Input voltage on any pin relative to ground:	-0.3V to V_{CC} + 0.3V
Maximum voltage:	8V
ESD protection on all pins:	>2000V

** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.*

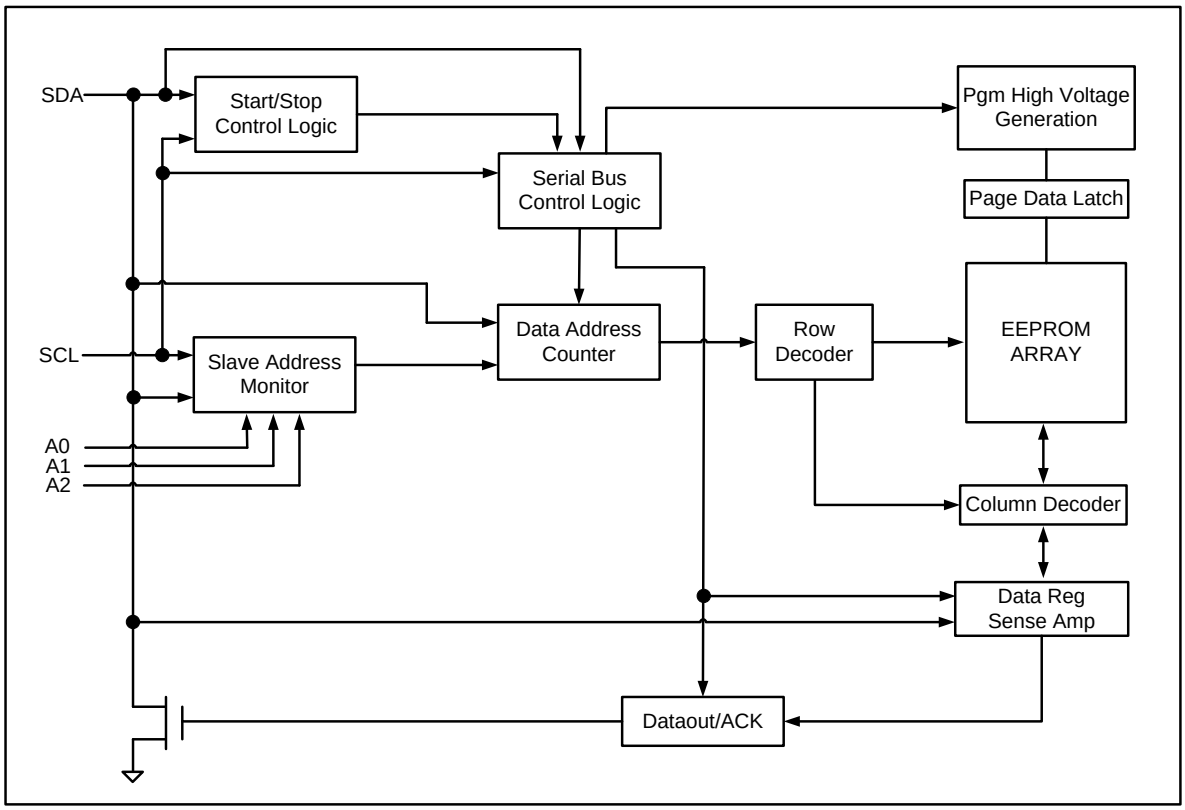


Figure 2: Block Diagram

PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) DEVICE / CHIP SELECT ADDRESSES (A2, A1, A0)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either V_{IH} or V_{IL}. If left unconnected, they are internally recognized as V_{IL}. However, due to capacitive coupling that may appear in customer applications, FMD recommends always connecting the address pins to a known state. When using a pull-up or pull-down resistor, FMD recommends using 10kΩ or less.

(C) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

DEVICE OPERATION

The FT34C04A operates as a slave device and utilizes a simple 2-wire digital serial interface, compatible with the I2C Fast-Mode Plus (I2C FM+) protocol, to communicate with a host controller, commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master, as well as, to send data back to the Master. Data is always latched into the FT34C04A on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise. All command and data information is transferred with the Most-Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data has been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices.The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.In order for the serial bus to be idle, both the SCL and SDA pins must be in the Logic 1 state at the same time.

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when

Serial clock SCL is at V_{IL}. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL $\geqslant V_{IH}$, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL $\geqslant V_{IH}$, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish.

(D) ACKNOWLEDGE (ACK)

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9th serial clock after each word.

(E) No-ACKNOWLEDGE (NACK)

When the FT34C04A is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a NACK response to the FT34C04A instead of an ACK response. This is accomplished by the Master outputting a Logic 1 during the ACK/NACK clock cycle, at which point the FT34C04A will release the SDA line so that the Master can then generate a Stop condition.

(F) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

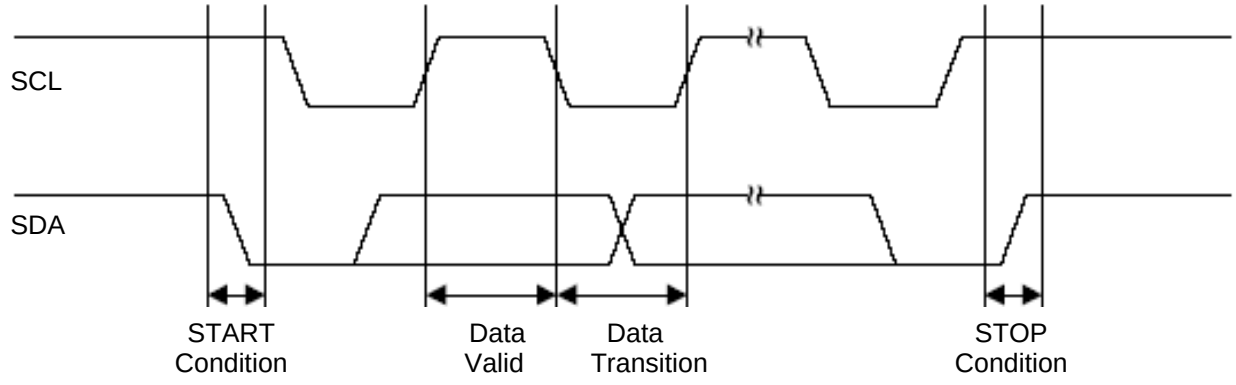


Figure 3: Timing diagram for START and STOP conditions

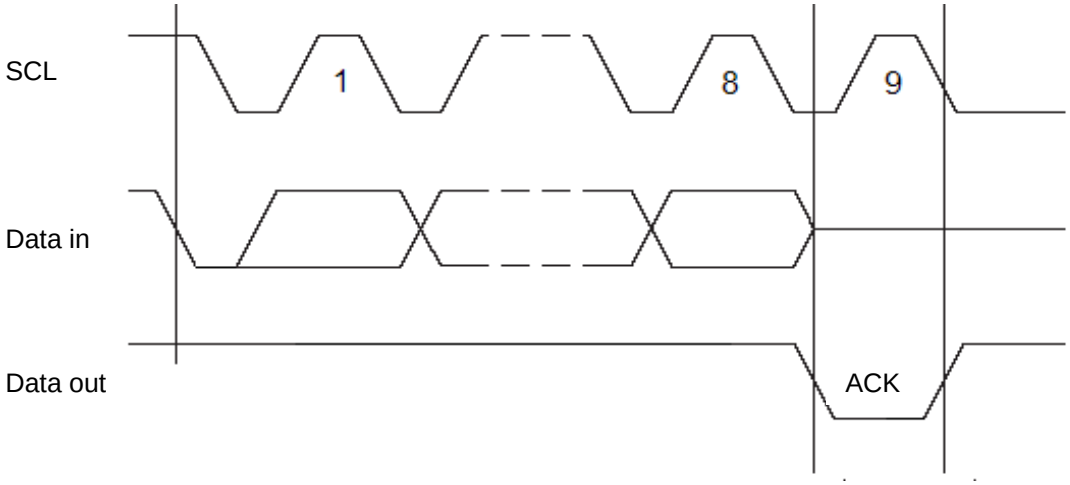


Figure 4: Timing diagram for output ACKNOWLEDGE

(G) Timeout Function

The FT34C04A supports the industry standard bus Timeout feature to help prevent potential system bus hangups.The device resets its serial interface and will stop driving the bus (will let SDA float high) if the SCL pin is held low for more than the minimum Timeout (t_{OUT}) specification. The FT34C04A will be ready to accept a new Start condition before the maximum t_{OUT} has elapsed . This feature does require a minimum SCL clock speed of 10kHz to avoid any timeout issues.

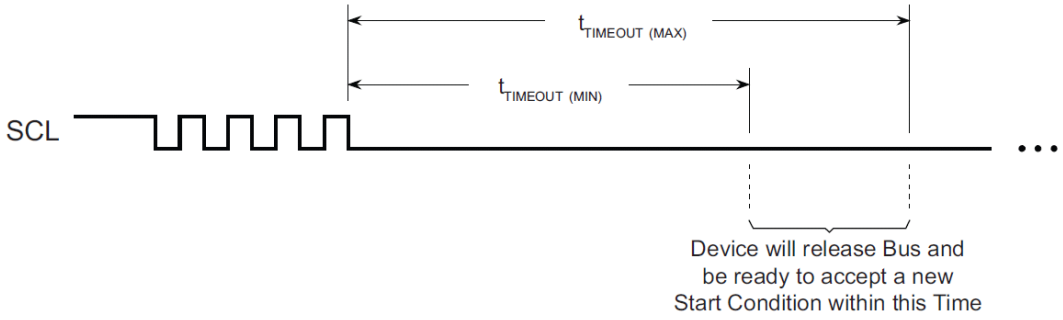


Figure 5: Timeout

(H) Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition.
2. Clock eighteen data bits “1”,.
3. Create another Start condition followed by Stop condition .

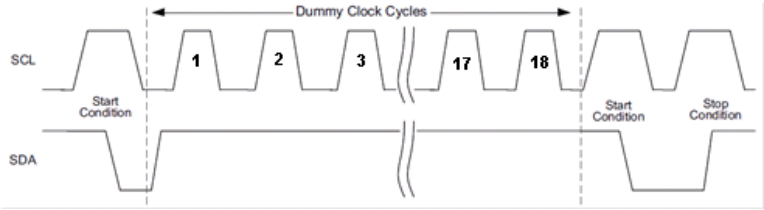


Figure 6: Software Reset

DEVICE ADDRESSING

The FT34C04A requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with the Serial EEPROM. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (A2, A1, and A0) and a R/W bit and is clocked by the Master on the SDA pin with the most significant bit first .The FT34C04A will respond to two unique device type identifiers. The device type identifier of '1010'(Ah) is necessary to select the device for reading or writing. The device type identifier of '0110'(6h) has multiple purposes. First, it is used to access the page address function which determines what the internal address counter is set to.The device type identifier of '0110'(6h) is also used to access the software write protection feature of the device.

Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Type Identifier				Device Address			Read/Write
EEPROM Read/Write	1	0	1	0	A2	A1	A0	R/$\overline{W}$
Write Protection and Page Address Functions	0	1	1	0	A2	A1	A0	R/$\overline{W}$

Table 2: Device Address Byte

The software device address bits (A2, A1, and A0) must match their corresponding hard-wired device address inputs (A2, A1 and A0) allowing up to eight devices on the bus at the same time. The eighth bit of the address byte is the R/W operation selection bit. A read operation is selected if this bit is a Logic 1, and a Write operation is selected if this bit is a Logic 0. Upon a compare of the device address byte, the FT34C04A will output an ACK during the ninth clock cycle; if a compare is not true, the device will output a NACK during the ninth clock cycle and return the device to the low-power Standby Mode.

Software Device Address Bits	Hard-wired Device Address Inputs		
A2, A1, A0	A_2	A_1	A_0
000	GND	GND	GND
001	GND	GND	V_{CC}
010	GND	V_{CC}	GND
011	GND	V_{CC}	V_{CC}
100	V_{CC}	GND	GND
101	V_{CC}	GND	V_{CC}
110	V_{CC}	V_{CC}	GND
111	V_{CC}	V_{CC}	V_{CC}

Table 3: Device Address Combinations

MEMORY ORGANIZATION

To provide the greatest flexibility and backwards compatibility with the previous generations of SPD devices, the FT34C04A memory organization is organized into two independent 2-Kbit memory arrays. Each 2-Kbit (256-byte) section is internally organized into two independent quadrants of 128 bytes with each quadrant comprised of eight pages of 16 bytes. Including both memory sections, there are four 128-byte quadrants totaling 512 bytes.

(A) Set Page Address and Read Page Address Commands

The FT34C04A incorporates an innovative memory addressing technique that utilizes a Set Page Address (SPA) and Read Page Address (RPA) commands to select and verify the desired half of the memory enabled to perform Write and Read operations. Due to the requirement for A0 pin to be driven to VHV, the SPA and the RPA commands are fully supported in a single DIMM (isolated DIMM) end application or a single DIMM programming station only.If SPA = 0, then the first-half or lower 256 bytes of the Serial EEPROM is selected allowing access to Quadrant 0 and Quadrant 1. Alternately, if SPA = 1, then the second-half or upper 256 bytes of the Serial EEPROM is selected allowing access to Quadrant 2 and Quadrant 3.

Block	Set Page Address (SPA)	Memory Address Locations
Quadrant 0	0	00h to 7Fh
Quadrant 1		80h to FFh
Quadrant 2	1	00h to 7Fh
Quadrant 3		80h to FFh

Table 4: SPA Setting and Memory Organization

Setting the Set Page Address (SPA) value selects the desired half of the EEPROM for performing Write or Read operations. This is done by sending the SPA as seen in Figure 6-1. The SPA command sequence requires the Master to transmit a Start condition followed by sending a control byte of ‘011011*0’ where the ‘*’ in the bit 7 position will dictate which half of the EEPROM is being addressed. A ‘0’ in this position (or 6Ch) is required to set the page address to the first half of the memory and a ‘1’ (or 6Eh) is necessary to set the page address to the second half of the memory. After receiving the control byte, the FT34C04A should return an ACK and the Master should follow by sending two data bytes of don’t care values. The FT34C04A responds with a NACK to each of these two data bytes although the JEDEC EE1004v specification allows for either an ACK or NACK response. The protocol is completed by the Master sending a Stop condition to end the operation.

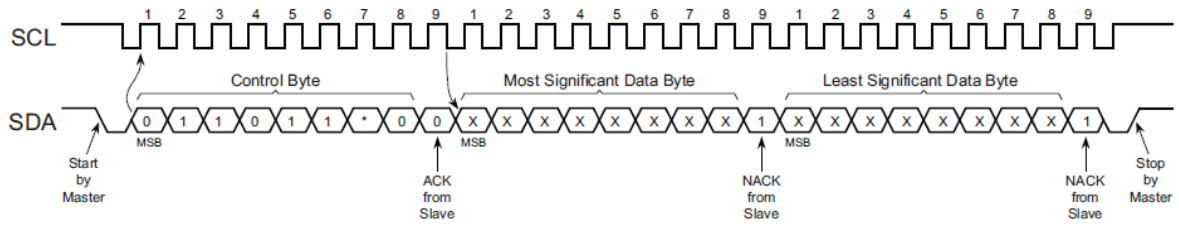


Figure 7: Set Page Address (SPA)

Reading the state of the SPA can be accomplished via the Read Page Address (RPA) command. The Master can issue the RPA command to determine if the FT34C04A’s internal address counter is

located in the first 2-Kbit section or the second 2-Kbit memory section based upon the device's ACK or NACK response to the RPA command.The RPA command sequence requires the Master to transmit a Start bit followed by a control byte of '01101101' (6Dh). If the device's current address counter (page address) is located in the first half of the memory, the FT34C04A responds with an ACK to the RPA command. Alternatively, a NACK response to the RPA command indicates the page address is located in the second half of the memory .Following the control byte and the device's ACK or NACK response, the FT34C04A should transmit two data bytes of don't care values. The Master should NACK on these two data bytes followed by the Master sending a Stop condition to end the operation. After power-up, the SPA is set to zero indicating internal address counter is located in the first half of the memory. Performing a software reset will also set the SPA to zero.The FT34C04A incorporates a Reversible Software Write Protect (RSWP) feature that allows the ability to selectively write protect data stored in any or all of the four 128-byte quadrants.

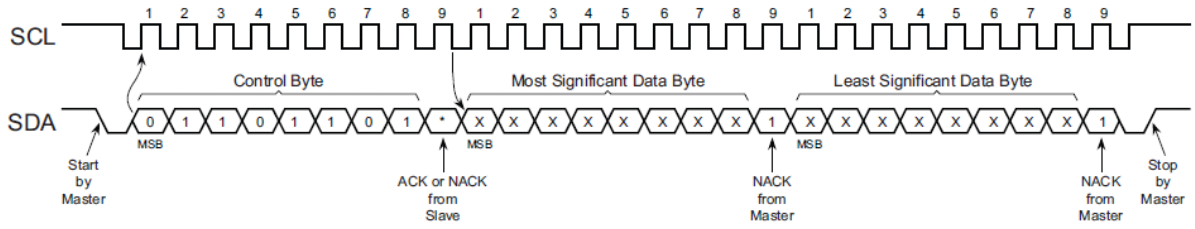


Figure 8: Read Page Address (RPA)

WRITE OPERATIONS

The FT34C04A supports single Byte Write and Page Write operations up to the maximum page size of 16 bytes in one operation. The only difference between a Byte Write and a Page Write operation is the amount of data bytes sent to the device. Regardless of whether a Byte Write or Page Write operation is performed, the internally self-timed write cycle will take the same amount of time to write the data to the addressed memory location(s). All Byte Write and Page Write operations should be preceded by the SPA and or RPA commands to ensure the internal address counter is located in the desired half of the memory. If a Byte Write or Page Write operation is attempted to a protected quadrant, the FT34C04A will respond (ACK or NACK) to the write operation according to Table 5.

Quadrant Status	Instruction	ACK	Word Address	ACK	Data Word	ACK	Write Cycle
Write Protected with Set RSWP	Set RSWP	NACK	Don't Care	NACK	Don't Care	NACK	No
	Clear RSWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write to Protected Quadrant	ACK	Word Address	ACK	Data	ACK	No
Not Protected	Set RSWP or Clear RSWP	ACK	Don't Care	ACK	Don't Care	ACK	Yes
	Byte Write or Page Write	ACK	Word Address	ACK	Data	ACK	Yes

Table 5: Acknowledge Status When Writing Data or Defining Write Protection

(A) BYTE WRITE

A byte write operation starts when a micro-controller sends a START bit condition, follows by a proper EEPROM device address and then a write command. If the device address bits match the chip select address, the EEPROM device will acknowledge at the 9th clock cycle. The micro-controller will then send the rest of the lower 8 bits word address. At the 18th cycle, the EEPROM will acknowledge the 8-bit address word. The micro-controller will then transmit the 8 bit data. Following an ACKNOWLDEGE signal from the EEPROM at the 27th clock cycle, the micro-controller will issue a STOP bit. After receiving the STOP bit, the EEPROM will go into a self-timed programming mode during which all external inputs will be disabled. After a programming time of T_{WC}, the byte programming will finish and the EEPROM device will return to the STANDBY mode.

(B) PAGE WRITE

A page write is similar to a byte write with the exception that one to sixteen bytes can be programmed along the same page or memory row. All FT34C04A are organized to have 16 bytes per memory row or page.

With the same write command as the byte write, the micro-controller does not issue a STOP bit after sending the 1st byte data and receiving the ACKNOWLEDGE signal from the EEPROM on the 27th clock cycle. Instead it sends out a second 8-bit data word, with the EEPROM acknowledging at the 36th cycle. This data sending and EEPROM acknowledging cycle repeats until the micro-controller sends a STOP bit after the n $\times$ 9th clock cycle. After which the EEPROM device will go into a self-timed partial or full page programming mode. After the page programming completes after a time of T_{WC}, the devices will return to the STANDBY mode.

The least significant 4 bits of the word address (column address) increments internally by one after receiving each data word. The rest of the word address bits (row address) do not change internally, but pointing to a specific memory row or page to be programmed. The first page write data word can be of any column address. Up to 16 data words can be loaded into a page. If more then 16 data words are loaded, the 9th data word will be loaded to the 1st data word column address. The 10th data word will be loaded to the 2nd data word column address and so on. In other word, data word address (column address) will “roll” over the previously loaded data.

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to “1”. The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8^{th}) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9^{th} serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. The address roll-over during a Read is from the last byte of the last page to the first byte of the first page of the addressed 2-Kbit (depends on the current SPA setting). For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18^{th} clock cycle. The micro-controller issues a valid STOP bit after the 18^{th} clock cycle to terminate the read operation. The device then returns to STANDBY mode.

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8^{th}) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9^{th} serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18^{th} clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27^{th} clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead.

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a "dummy write" instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8^{th}) set to "0". The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address.

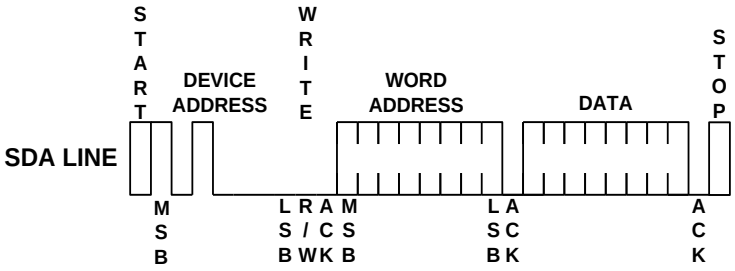


Figure 9: Byte Write

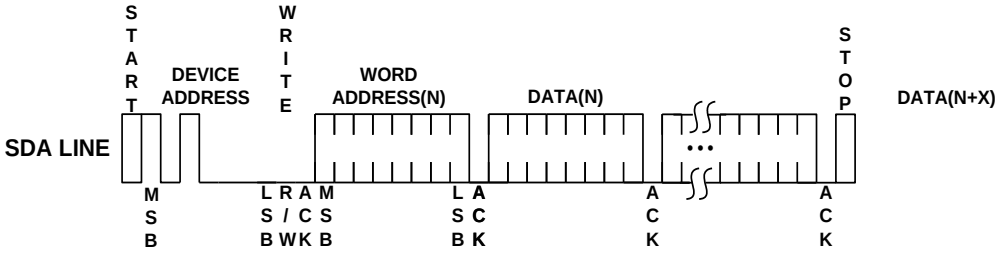


Figure 10: Page Write

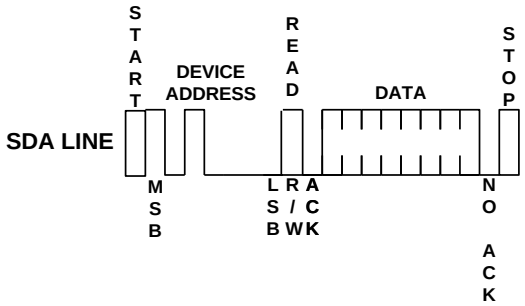


Figure11: Current Address Read

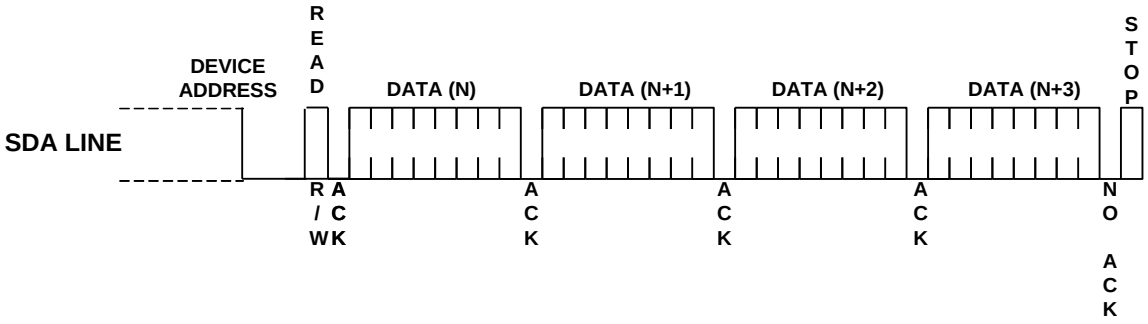


Figure 12: Sequential Read

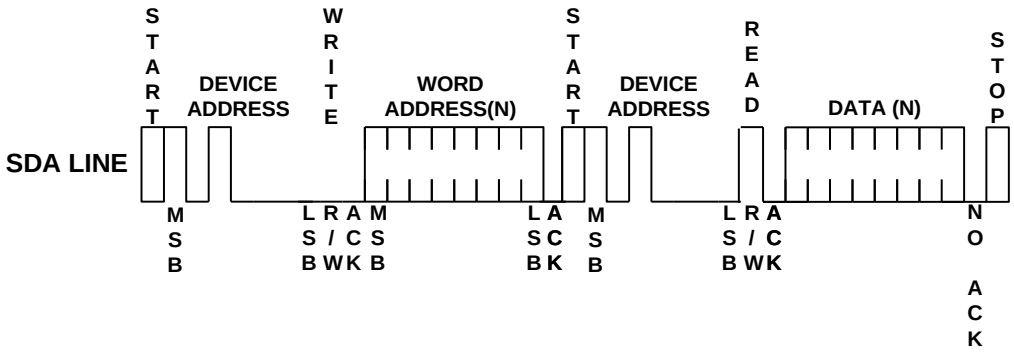


Figure 13: Random Read

Write Protection

The FT34C04A incorporates a Reversible Software Write Protection (RSWP) feature that allows the ability to selectively write protect data stored in each of the four independent 128-byte EEPROM quadrants. Table 6 identifies the memory quadrant identifier with its associated quadrant, SPA and memory address locations.

Block	Set Page Address (SPA)	Memory Address Locations
Quadrant 0	0	00h to 7Fh
Quadrant 1		80h to FFh
Quadrant 2	1	00h to 7Fh
Quadrant 3		80h to FFh

Table 6: Memory Organization

(A) Set RSWP

Setting the RSWP is enabled by sending the Set RSWP command, similar to a normal Write command to the device which programs the write protection to the target quadrant. The Set RSWP sequence requires sending a control byte of '0110MMM0' (where 'M' represents the memory quadrant identifier for the target quadrant to be write-protected) with the R/W bit set to a Logic 0. In conjunction with sending the protocol, the A0 pin must be connected to V_{HV} for the duration of the RSWP sequence. The Set RSWP command acts on a single quadrant only as specified in the Set RSWP command and can only be reversed by issuing the Clear RSWP command and will unprotect all quadrants in one operation .

Function	Pin			Control Byte							
				Device Type Identifier				Memory Quadrant Identifier			R/$\overline{W}$
	A_2	A_1	A_0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Set RSWP, Quadrant 0	X	X	V_{HV}	0	1	1	0	0	0	1	0
Set RSWP, Quadrant 1	X	X						1	0	0	0
Set RSWP, Quadrant 2	X	X						1	0	1	0
Set RSWP, Quadrant 3	X	X						0	0	0	0
Clear RSWP	X	X						0	1	1	0

Table 7: Set RSWP and Clear RSWP

X = Don't care but recommended to be hard-wired to VCC or GND.

Due to the requirement for the A0 pin to be driven to V_{HV}, the RSWP set and RSWP clear commands are fully supported in a single DIMM (isolated DIMM) end application or a single DIMM programming station only.

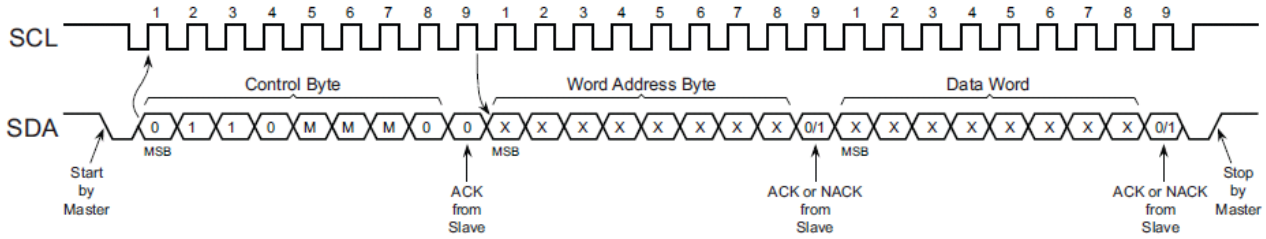


Figure 14: Set RSWP and Clear RSWP

X = Don't care

(B) Clear RSWP

Similar to the Set RSWP command, the reversible write protection on all quadrants can be reversed or unprotected by transmitting the Clear RSWP command. The Clear RSWP sequence requires the Master to send a Start condition followed by sending a control byte of '01100110'(66h) with the R/W bit set to a Logic 0. The FT34C04A should respond with an ACK. The Master transmits a word address byte and data bytes with don't care values. The FT34C04A will respond with either an ACK or NACK to both the word address and data word. In conjunction with sending the protocol, the A0 pin must be connected to V_{HV} for the duration of the Clear RSWP command. To end the Clear RSWP sequence, the Master sends a Stop condition.

(C) Read RSWP

The Read RSWP command allows the ability to check a quadrant's write protection status. To find out if the software write protection has been set to a specific quadrant, the same procedure that was used to set the quadrant's write protection can be utilized except that the R/W select bit is set to a Logic 1, and the A0 pin is not required to have V_{HV}.The Read RSWP sequence requires sending a control byte of '0110MMM1' (where the 'M' represents the memory quadrant identifier for the quadrant to be read) with the R/W bit set to a Logic 1 .If the RSWP has not been set, then the FT34C04A responds to the control byte with an ACK. If the RSWP has been set, the FT34C04A responds with a NACK. In either case, both Word Address and Data Word bytes will not be acknowledged. The operation is completed by the Master creating a Stop Condition.

Quadrant Status	Instruction Sent	Instruction Response	Word Address Sent	Word Address Response	Data Word Sent	Data Word Response
Write Protected	Read RSWP	NACK	Don't Care	NACK	Don't Care	NACK
Not Protected	Read RSWP	ACK	Don't Care	NACK	Don't Care	NACK

Table 8: Acknowledge When Reading Protection Status

Function	Pin			Control Byte							
				Device Type Identifier				Memory Quadrant Identifier			R/$\overline{W}$
	A_2	A_1	A_0	B7	B6	B5	B4	B3	B2	B1	B0
Read RSWP, Quadrant 0	X	X	0, 1	0	1	1	0	0	0	1	1
Read RSWP, Quadrant 1	X	X						1	0	0	1

Read RSWP, Quadrant 2	X	X	or					1	0	1	1
Read RSWP, Quadrant 3	X	X	V_{HV}					0	0	0	1

Table 9: Read RSWP

X = Don't care

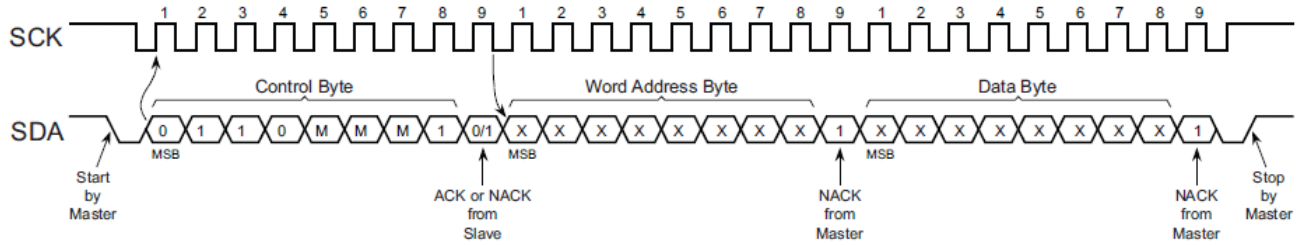


Figure 15: Read RSWP

X = Don't care

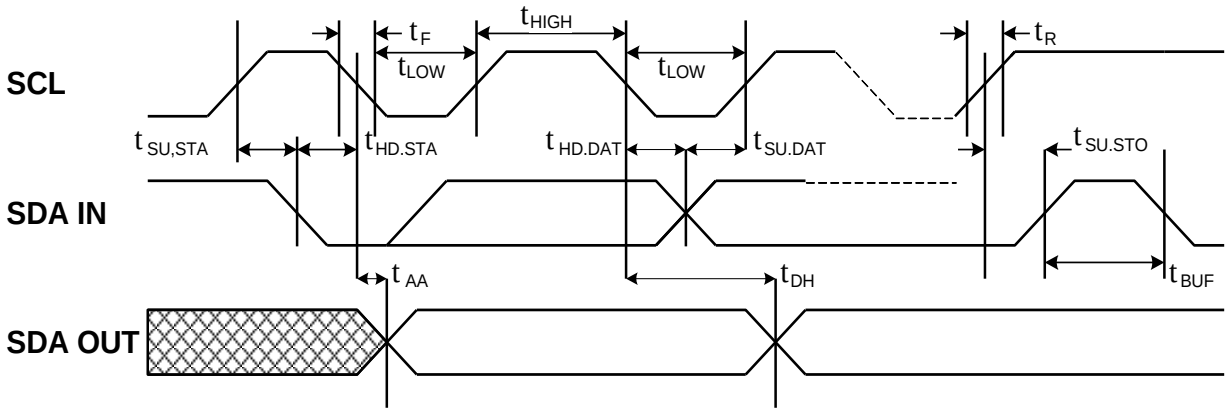


Figure 16: SCL and SDA Bus Timing

Electrical Specifications

(A)Power-Up Requirements

During a power-up sequence, the VCC supplied to the device should monotonically rise from GND to the minimum VCC level, with a slew rate no faster than 0.05 V/μs and no slower then 0.1 V/ms. A decoupling cap should be connected to the VCC PAD which is no smaller than 10nF.

(B)Device Reset

To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, this device includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any commands until the VCC level crosses the internal voltage threshold (V_{POR}) that brings the device out of Reset and into Standby mode. The system designer must ensure the instructions are not sent to the device until the VCC supply has reached a stable value greater than or equal to the minimum VCC level.

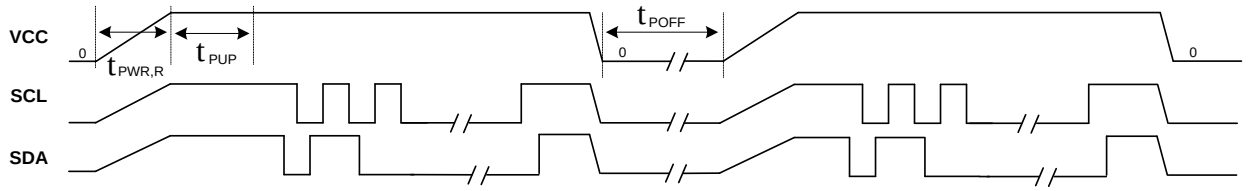


Figure 17: Power on and Power down

If an event occurs in the system where the VCC level supplied to the device drops below the maximum V_{POR} level specified, it is recommended that a full power cycle sequence be performed by first driving the VCC pin to GND, waiting at least the minimum t_{POFF} time and then performing a new power-up sequence in compliance with the requirements defined in this section.

AC CHARACTERISTICS

Symbol	Parameter	VCC < 2.2V		VCC ≥ 2.2V				Units
		100kHz		400kHz		1000kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10(2)	100	10(2)	400	10(2)	1,000	kHz
t_{LOW}	Clock Pulse Width Low	4,700		1,300		500		ns
t_{HIGH}	Clock Pulse Width High	4,000		600		260		ns
t_I	Noise Suppression Time		50		50		50	ns
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4,700		1,300		500		ns
$t_{HD.STA}$	Start Hold Time	4,000		600		260		ns
$t_{SU.STA}$	Start Set-up Time	4,700		600		260		ns
$t_{HD.DI}$	Data In Hold Time	0.0		0.0		0.0		ns
$t_{SU.DAT}$	Data In Set-up Time	250		100		50		ns
t_R	Inputs Rise Time(1)		1,000	20	300		120	ns
t_F	Inputs Fall Time(1)		300	20	300		120	ns
$t_{SU.STO}$	Stop Set-up Time	4,000		600		260		ns
$t_{HD.DAT}$	Data Out Hold Time	200	3,450	200	900	0	350	ns
$t_{PWR,R}$(1)	Vcc slew rate at power up	0.1	50	0.1	50	0.1	50	V/ms
t_{PUP}(1)	Time required after VCC is stable before the device can accept commands	100		100		100		µs
t_{POFF}(1)	Minimum time at Vcc=0V between power cycles	500		500		500		ms
t_{WR}	Write Cycle Time		5		5		5	ms
t_{OUT}	Timeout Time	25	35	25	35	25	35	ms
Endurance	25°C, Page Mode(1)	1,000,000						Write Cycles

Notes: 1. This Parameter is expected by characterization but is not fully screened by test.

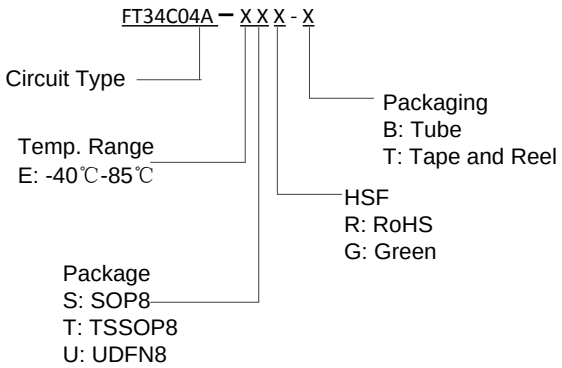
2. The minimum frequency is specified at 10kHz to avoid activating the timeout feature.

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			1.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V	Read at 100kHz			1.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V	Write at 100kHz			3.0	mA
I_{SB}	Standby Current	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		< 3.0		μA
		V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}		< 4.0		μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}				2.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}				2.0	μA
V_{IL}	Input Low Level(1)			-0.5		0.3 * V_{CC}	V
V_{IH}	Input High Level(1)			0.7 * V_{CC}		V_{CC} + 0.5	V
V_{OL1}	Low-Level Output Voltage Open-Drain	V_{CC} > 2V	I_{OL} = 3mA			0.4	V
V_{OL2}		V_{CC} ≤ 2V	I_{OL} = 2mA			0.2 * V_{CC}	V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4V	Freq ≤ 400kHz	3.0			mA
		V_{OL} = 0.6V	Freq ≤ 400kHz	6.0			mA
		V_{OL} = 0.4V	Freq > 400kHz	20.0			mA
V_{HV}	A_0 Pin High Voltage	V_{HV} - V_{CC} ≥ 4.8V		7		10	V
V_{HYST1}	Input Hysteresis (SDA, SCL)	V_{CC} < 2V		0.10 * V_{CC}			V
V_{HYST2}	Input Hysteresis (SDA, SCL)	V_{CC} ≥ 2V		0.05 * V_{CC}			V

DC CHARACTERISTICS

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

ORDER CODE:

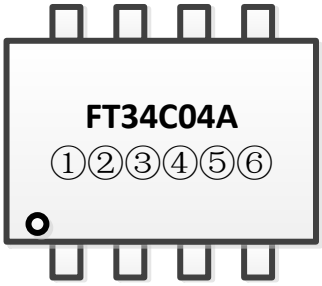


ORDER INFORMATION

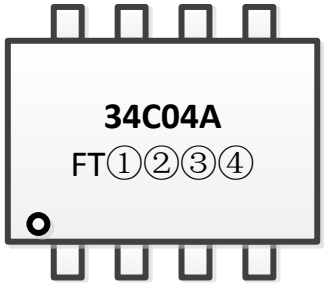
Package	Temperature Range	Vcc	HSF	Packaging	Order code
SOP8	-40℃-85℃	1.7V-3.6V	RoHS	Tube	FT34C04A-ESR-B
				Tape and Reel	FT34C04A-ESR-T
			Green	Tube	FT34C04A-ESG-B
				Tape and Reel	FT34C04A-ESG-T
TSSOP8	-40℃-85℃	1.7V-3.6V	RoHS	Tube	FT34C04A-ETR-B
				Tape and Reel	FT34C04A-ETR-T
			Green	Tube	FT34C04A-ETG-B
				Tape and Reel	FT34C04A-ETG-T
UDFN8	-40℃-85℃	1.7V-3.6V	RoHS	Tape and Reel	FT34C04A-EUR-T
			Green	Tape and Reel	FT34C04A-EUG-T

MARKING RULE

UDFN



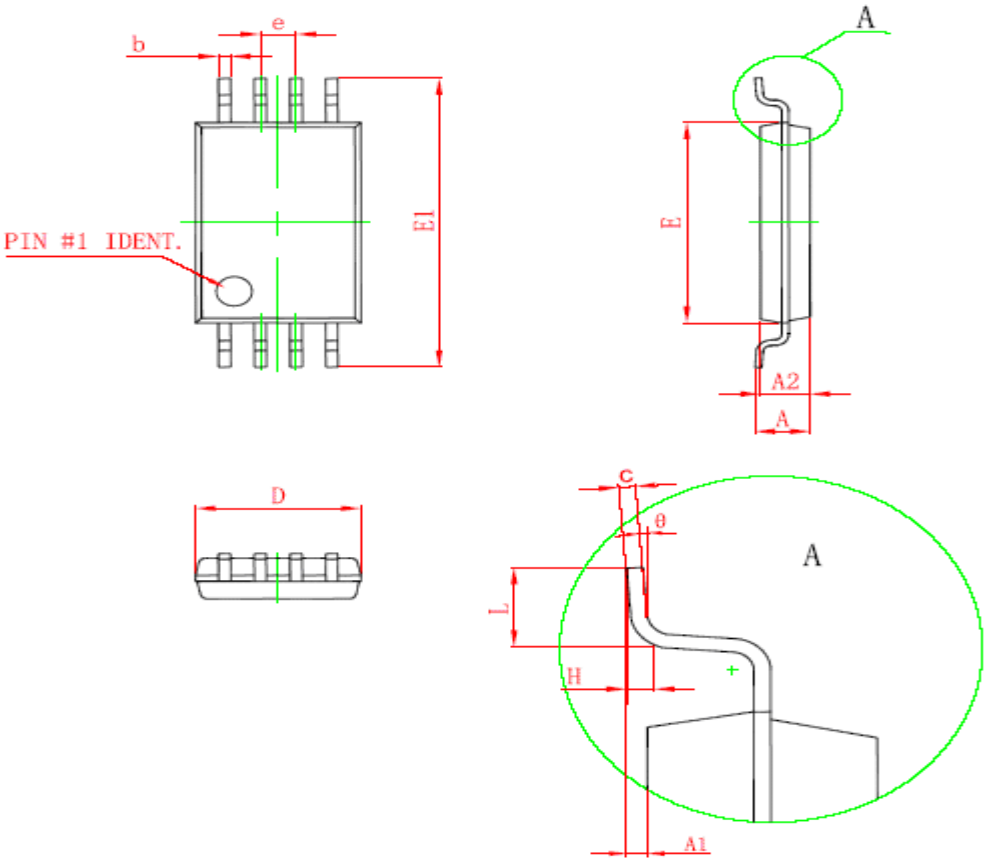
SOP8



TSSOP8

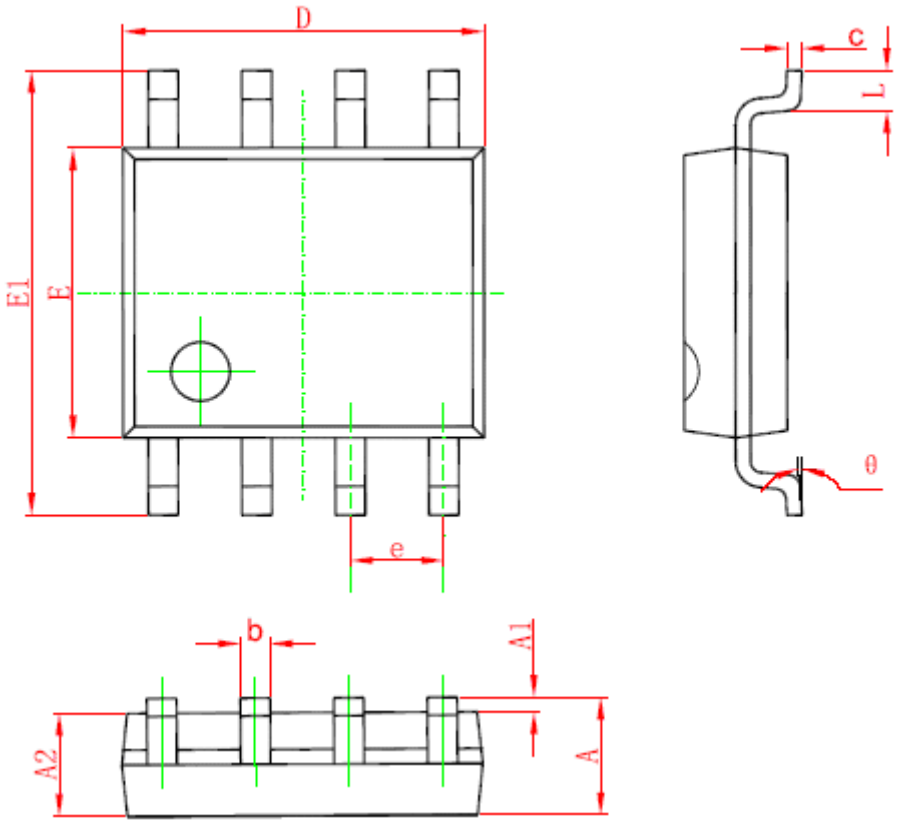
①②③④⑤⑥ for internal reference

TSSOP8 PACKAGE OUTLINE DIMENSIONS



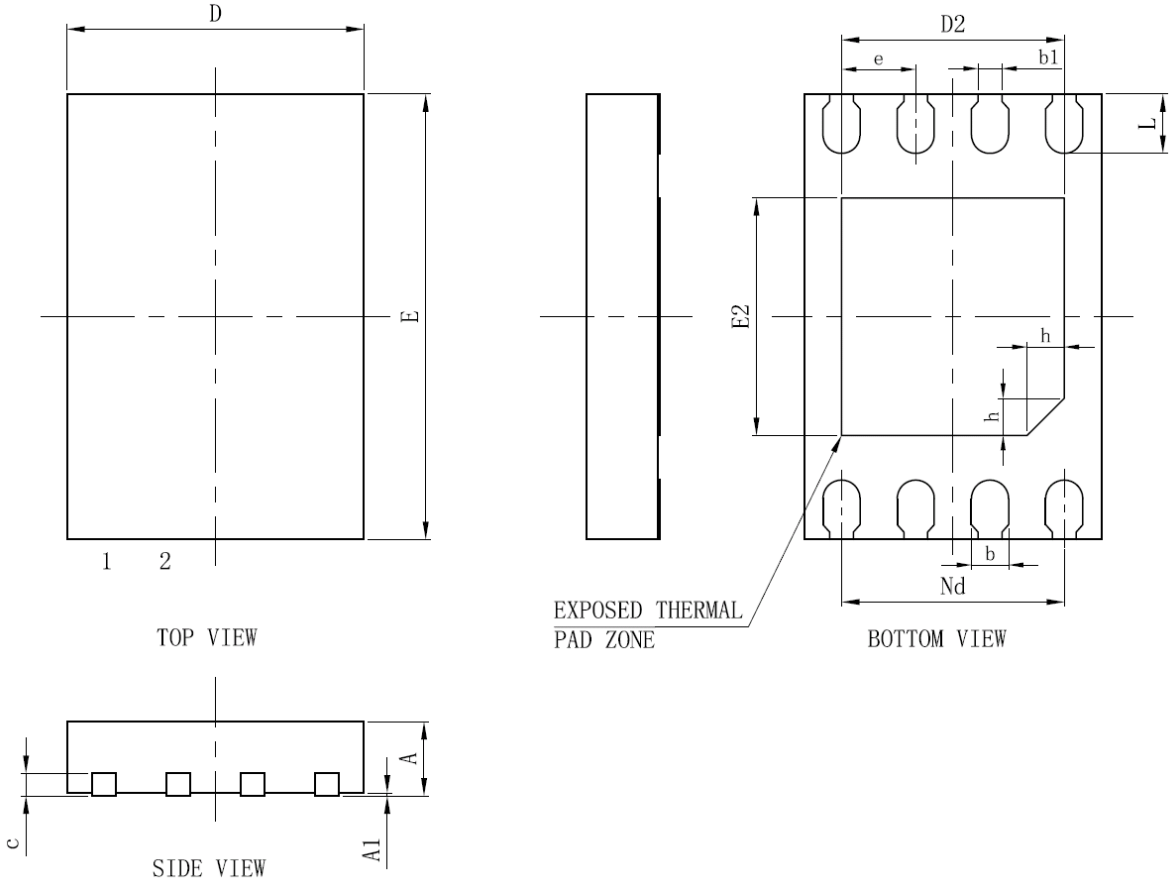
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

UDFN8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.017	0.021
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.039
b1	0.160REF		0.006REF	
c	0.100	0.200	0.004	0.008
D	1.900	2.100	0.075	0.083
D2	1.400	1.600	0.055	0.062
e	0.500BSC		0.020BSC	
Nd	1.500BSC		0.059BSC	
E	2.900	3.100	0.114	0.122
E2	1.500	1.700	0.059	0.067
L	0.300	0.500	0.012	0.020
h	0.200	0.300	0.066	0.12

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